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OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
GERSTL, SHANE F	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 03/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/818,910	GOTO, HARUTAKA	
	Examiner	Art Unit	
	Shane F Gerstl	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 have been examined.

Papers Received

2. Receipt is acknowledged of amendment papers submitted, where the papers have been placed of record in the file.

3. The amendment filed 14 February 2005 has successfully overcome the objection to the title and some of the 35 USC 112 rejections, which are herein withdrawn. The remaining 35 USC 112 claim rejections have been maintained as given below along with a new rejection.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Claims 1 and 9 recite the limitation "said control signal" in lines 7 and 11-12 of the claims. There is insufficient antecedent basis for this limitation in the claim. Lines 5-6 of the claims define a plurality of control signals. The examiner is taking the claims to mean “said control signals” in each instance in order to conform to that set forth in the amendment.

7. Similarly Claims 1 and 9 recite the limitations “the corresponding control signal” in lines 9-10 when previously corresponding control signals in the plural have been

defined. The examiner is taking the phrase to mean "the corresponding control signals" as fits the context of the claims.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-2, 5-10, and 13-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Sanders (5,006,980).

10. In regard to claim 1, Sanders discloses a data processing apparatus configured to perform a pipeline processing by dividing a pipeline into a plurality of stages, comprising:

a. a first pipeline processing portion configured to perform the processing in a plurality of stages in sequence based on a plurality of control signals provided corresponding to the respective stages, said control signals having timings capable of being individually controlled; [Column 5, lines 31-37 show that there are two pipelines with the first being an execution unit pipeline that processes calculations on operands. Figure 12 shows this sequential execution unit pipeline. Column 6, lines 66-68 show that there is a control input (signal), 28, to this execution unit pipeline. Figure 12 also shows this control signal, 28, and that

it is divided into multiple control signals and sent through latches (165-167) input to each stage of the first pipeline. The figure shows that the timings of each of these control signals is individually controlled by a corresponding latch, which has a clock input. Though the origin of the control signals for the execution unit and memory management units is the same (i.e. signal 28) and the values may initially be the same when split to the two units, the fact that the signal 28 is split defines the existence of two control signals, which are then separately and individually controlled in the following stages as shown in figure 12.]

b. a first latch portion configured to latch said control signals inputted to each stage with a predetermined clock, said first latch portion having a plurality of flip-flops which are provided corresponding to the respective control signals and latch the corresponding control signal; [Figure 12, elements 165-170 make up a first latch portion. The figure shows that this latch portion latches the control signals input to each stage with a clock signal. Figure 12 clearly shows that the control input 28 is latched based on a clock signal (which is inherently predetermined, that is determined before it is asserted) in each stage. Thus operation, while dependent on the data of the control signals originating from signal 28, is dependent on the timings of the clock signals. In certain stages such as segment 4 the clock signals are shown to be separate and different. Since the latch is timed according to a clock signal, the latch is a flip-flop.]

c. and a second pipeline processing portion, disposed separately from said first pipeline processing portion, configured to perform the processing in each

stage based on the control signal latched by said first latch portion. [Column 5, lines 31-37 show that the second pipeline processing portion is a memory request pipeline that calculates addresses and fetches operands. Figure 12, shows this memory request (memory management unit) pipeline. Column 7, lines 5-7 show that this memory management unit pipeline is controlled by control signals. The figure also shows that the control signals latched by the first portion as, described above, is sent to each stage to control the processing there.]

11. In regard to claim 2, Sanders discloses the data processing apparatus according to claim 1, wherein said control signal is a signal for controlling whether or not the pipeline processing is stalled. [Column 17, lines 34-37 show that on a stall, the latching portion is deasserted and the control signal does not proceed. If the control signal does not proceed, processing stops. Therefore, the control signal controls whether the processing is stalled based on if it proceeds or not.]

12. In regard to claim 5, Sanders discloses the data processing apparatus according to claim 1, wherein said latch portion latches said control signal with a clock for dividing the respective stages. [As shown above, the latch latches the control with a clock signal. As can be seen from figure 12, there is one latch per stage, therefore, the stages are divided by latching the control signals with the clock signal.]

13. In regard to claim 6, Sanders discloses the data processing apparatus according to claim 1, wherein said second pipeline processing portion performs the pipeline processing later by one cycle or more later than a clock for discriminating the stages of

said first pipeline processing portion. [Column 5, lines 31-37 show that the execution and memory pipelines execute in lock step and thus for example segment-3 of both pipelines proceed at the same time. As can be seen from figure 12, segment-4 of the memory management unit pipeline performs pipeline processing in the memory pipeline one cycle later than segment-3 in the execution unit pipeline and thus one cycle later than the clock pulse received at segment-3.]

14. In regard to claim 7, Sanders discloses the data processing apparatus according to claim 1, wherein said second pipeline processing portion performs the pipeline processing one cycle or less than a clock for dividing the stages of said first pipeline processing portion. [Column 5, lines 31-37 show that the execution and memory pipelines execute in lock step and thus for example segment-3 of both pipelines proceed at the same time. As can be seen from figure 12, segment-3 performs pipeline processing in the memory pipeline less than one cycle later, in fact zero cycles later, than segment-3 in the execution unit pipeline and the clock controlling it.]

15. In regard to claim 8, Sanders discloses the data processing apparatus according to claim 1, wherein one of said first and second pipeline processing portions includes an integer operation unit, and the other includes an operation unit other than the integer operation unit; [Figure 2 shows that the execution unit pipeline includes an arithmetic and logic unit (ALU) and a shift unit. It is well known to one of ordinary skill in the art that these units are inherently integer operation units. As shown previously, the other pipeline is a memory management pipeline and thus includes other than an integer unit.]

16. In regard to claim 9, Sanders discloses a data processing method for performing first and second pipeline processings by dividing a pipeline into a plurality of stages, comprising steps of:

a. performing said first pipeline processing in a plurality of stages in sequence based on a plurality of control signals provided corresponding to the respective stages, said control signals having timings capable of being individually controlled; [Column 5, lines 31-37 show that there are two pipelines with the first being an execution unit pipeline that processes calculations on operands. Figure 12 shows this sequential execution unit pipeline. Column 6, lines 66-68 show that there is a control input (signal), 28, to this execution unit pipeline. Figure 12 also shows this control signal, 28, and that it is divided into multiple control signals and sent through latches (165-167) input to each stage of the first pipeline. The figure shows that the timings of each of these control signals is individually controlled by a corresponding latch, which has a clock input. Though the origin of the control signals for the execution unit and memory management units is the same (i.e. signal 28) and the values may initially be the same when split to the two units, the fact that the signal 28 is split defines the existence of two control signals, which are then separately and individually controlled in the following stages as shown in figure 12.]

b. performing a first latch processing to latch said control signals inputted to each stage with a predetermined clock; [Figure 12, elements 165-170 make up a first latch portion. The figure shows that this latch portion latches the control

signals input to each stage with a clock signal. Figure 12 clearly shows that the control input 28 is latched based on a clock signal (which is inherently predetermined, that is determined before it is asserted) in each stage. Thus operation, while dependent on the data of the control signals originating from signal 28, is dependent on the timings of the clock signals. In certain stages such as segment 4 the clock signals are shown to be separate and different. Since the latch is timed according to a clock signal, the latch is a flip-flop.]

c. and a second pipeline processing (using figure 1, elements 10-13), based on said latched control signals separately from said first pipeline processing. [Column 5, lines 31-37 show that the second pipeline processing portion is a memory request pipeline that calculates addresses and fetches operands. Figure 12, shows this memory request (memory management unit) pipeline. Column 7, lines 5-7 show that this memory management unit pipeline is controlled by control signals. The figure also shows that the control signals latched by the first portion as, described above, is sent to each stage to control the processing there.]

17. In regard to claim 10, Sanders discloses the data processing method according to claim 9, wherein said control signal is a signal for controlling whether or not the pipeline processing is stalled. [Column 17, lines 34-37 show that on a stall, the latching portion is deasserted and the control signal does not proceed. If the control signal does not proceed, processing stops. Therefore, the control signal controls whether the processing is stalled based on if it proceeds or not.]

18. In regard to claim 13, Sanders discloses the data processing method according to claim 9, wherein said first latch processing comprises a step of latching said control signal with a clock for discriminating the respective stages. [As shown above, the latch latches the control with a clock signal. As can be seen from figure 12, there is one latch per stage, therefore, the stages are divided by latching the control signals with the clock signal.]

19. In regard to claim 14, Sanders discloses the data processing method according to claim 9, wherein said second pipeline processing performs the pipeline processing later by one cycle or more later than a clock for discriminating the stages of said first pipeline processing. [Column 5, lines 31-37 show that the execution and memory pipelines execute in lock step and thus for example segment-3 of both pipelines proceed at the same time. As can be seen from figure 12, segment-4 of the memory management unit pipeline performs pipeline processing in the memory pipeline one cycle later than segment-3 in the execution unit pipeline and thus one cycle later than the clock pulse received at segment-3.]

20. In regard to claim 15, Sanders discloses the data processing method according to claim 9, wherein said second pipeline processing performs the pipeline processing later by less than one cycle or less than a clock for discriminating the stages of said first pipeline processing. [Column 5, lines 31-37 show that the execution and memory pipelines execute in lock step and thus for example segment-3 of both pipelines proceed at the same time. As can be seen from figure 12, segment-3 performs pipeline

processing in the memory pipeline less than one cycle later, in fact zero cycles later, than segment-3 in the execution unit pipeline and the clock controlling it.]

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. Claims 3, 4, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sanders in view of Gearty (6,477,638) and further in view of Hennessy.

23. In regard to claim 3,

a. Sanders discloses the data processing apparatus according to claim 1,

b. Sanders does not disclose the apparatus further comprising second latch portion configured to latch a processing result in at least one stage in said first pipeline processing portion with said predetermined clock, wherein said second pipeline processing portion utilizes data latched by said second latch portion to perform the processing in the stage corresponding to the data latched by said second latch portion.

c. Gearty has disclosed a dual-pipelined apparatus comprising second latch portion (figure 4, element 174C) configured to latch a processing result in at least one stage (figure 4, stage E3) in said first pipeline processing portion (figure 4, element 160) with said predetermined clock, wherein said second pipeline

processing portion (figure 4, element 162) utilizes data latched by said second latch portion to perform the processing in the stage corresponding to the data latched by said second latch portion. The figure shows this latch to hold ifu_fpu_data_wb. Table 1 of columns 7 and 8 shows that this signal comprises 64 bits as a result from the CPU (first) pipeline and is used by the F4 stage in the second pipeline for processing an FLD or FMOV instruction. One of ordinary skill in the art would recognize that latch 174C is latched with a clock due to the triangular shape drawn on its lower portion with further support of this in column 5, line 66 – column 7, line 4.

d. One can see that from figure 4 of Gearty, the data from the first pipeline is being sent or forwarded to the second pipeline. Thus, the second pipeline does not have to retrieve this data from memory or calculate it. Hennessy has shown on page 445 in the bottom paragraph that this forwarding allows for the retrieval of a missing or needed item early. The ability to retrieve a data item early in order to save time would have motivated one of ordinary skill in the art to change the design of Sanders to use the forwarding methodology taught by Gearty.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Sanders to include the data-forwarding scheme taught by Gearty so that data items may be received early in order to save time as taught by Hennessy.

24. In regard to claim 4,

a. Sanders discloses the data processing apparatus according to claim 1,

b. Sanders does not disclose the apparatus further comprising:

i. a third latch portion configured to latch a processing result in at least one stage in said second pipeline processing portion with said predetermined clock;

ii. and a selector configured to select either one of data before latched by said third latch portion and data latched by said third latch portion,

iii. wherein said selector selects a latch output of said third latch portion after the completion of stall, if said first pipeline processing portion is stalled when the processing result in said second pipeline processing portion is transmitted to said first pipeline processing portion, and selects the processing result in said second pipeline processing portion, when said first pipeline processing portion is not stalled.

c. Gearty discloses a dual-pipelined apparatus further comprising:

i. a third latch portion (figure 7, element 290) configured to latch a processing result in at least one stage (figure 7, stage F1) in said second pipeline (figure 7, right pipeline, and figure 4, element 162) processing portion with said predetermined clock; Column 13, lines 29-30 and Table 1 show that a data signal (processing result) is sent on line 302 and then to the third latch portion as shown as the figure. One of ordinary skill in the art would recognize that latch 174C is latched with a clock due to the triangular shape drawn on its lower portion with further support of this in column 5, line 66 – column 7, line 4.

ii. and a selector (figure 12, element 296, and column 13, lines 29-30) configured to select either one of data before latched by said third latch portion and data latched by said third latch portion (as shown in the figure),

iii. wherein said selector selects a latch output of said third latch portion after the completion of stall, if said first pipeline processing portion is stalled when the processing result in said second pipeline processing portion is transmitted to said first pipeline processing portion, and selects the processing result in said second pipeline processing portion, when said first pipeline processing portion is not stalled. Column 13, lines 14-35 show that when the first pipeline is stalled, the aforementioned third latch stores the data to be transmitted to it and when the stall is complete, the selector selects the data from the latch and transmits it to the first pipeline.

d. One can see that from figures 4 and 7 of Gearty, the data from the second pipeline is being sent or forwarded to the first pipeline. Thus, the first pipeline does not have to retrieve this data from memory or calculate it. Hennessy has shown on page 445 in the bottom paragraph that this forwarding allows for the retrieval of a missing or needed item early. The ability to retrieve a data item early in order to save time would have motivated one of ordinary skill in the art to change the design of Sanders to use the forwarding methodology taught by Gearty.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Sanders to include the data-forwarding scheme taught by Gearty so that data items may be received early in order to save time as taught by Hennessy.

25. In regard to claim 11,

a. Sanders discloses the data processing method according to claim 1,

b. Sanders does not disclose the method further comprising a step of performing a second latch processing to latch a processing result in at least one stage in said first pipeline processing with said predetermined clock, wherein said second pipeline processing comprises a step of utilizing data latched by said second latch processing, when performing the processing in the stage for the data latched by said second latch processing.

c. Sanders does not disclose the method further comprising a step of performing a second latch processing to latch a processing result (using figure 4, element 174C) in at least one stage (figure 4, stage E3) in said first pipeline processing (using figure 4, element 160) with said predetermined clock, wherein said second pipeline processing (using figure 4, element 162) comprises a step of utilizing data latched by said second latch processing, when performing the processing in the stage for the data latched by said second latch processing. The figure shows this latch processing to hold ifu_fpu_data_wb. Table 1 of columns 7 and 8 shows that this signal comprises 64 bits as a result from the CPU (first) pipeline and is used by the F4 stage in the second pipeline for processing an FLD or FMOV instruction. One of ordinary skill in the art would

recognize that latch 174C is latched with a clock due to the triangular shape drawn on its lower portion with further support of this in column 5, line 66 – column 7, line 4.

d. One can see that from figure 4 of Gearty, the data from the first pipeline is being sent or forwarded to the second pipeline. Thus, the second pipeline does not have to retrieve this data from memory or calculate it. Hennessy has shown on page 445 in the bottom paragraph that this forwarding allows for the retrieval of a missing or needed item early. The ability to retrieve a data item early in order to save time would have motivated one of ordinary skill in the art to change the design of Sanders to use the forwarding methodology taught by Gearty.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Sanders to include the data-forwarding scheme taught by Gearty so that data items may be received early in order to save time as taught by Hennessy.

26. In regard to claim 12,

a. Sanders discloses the data processing method according to claim 9,

b. Sanders does not disclose the method further comprising steps of:

i. Performing a third latch processing to latch a processing result in at least one stage in said second pipeline processing with said predetermined clock;

ii. and selecting either one of data before latched by said third latch processing and data latched by said third latch processing,

iii. wherein said selecting step includes steps of: selecting a latch output of said third latch processing after the completion of stall; and selecting the processing result in said second pipeline processing, when said first pipeline processing is not stalled.

c. Gearty discloses a dual-pipelined processing further comprising:

i. Performing a third latch processing to latch a processing result (using figure 7, element 290) in at least one stage (figure 7, stage F1) in said second pipeline processing (using figure 7, right pipeline, and figure 4, element 162) with said predetermined clock; Column 13, lines 29-30 and Table 1 show that a data signal (processing result) is sent on line 302 and then to the third latch portion as shown as the figure. One of ordinary skill in the art would recognize that latch 174C is latched with a clock due to the triangular shape drawn on its lower portion with further support of this in column 5, line 66 – column 7, line 4.

ii. and selecting (using figure 12, element 296, and column 13, lines 29-30) either one of data before latched by said third latch processing and data latched by said third latch processing (as shown in the figure),

iii. wherein said selecting step includes steps of: selecting a latch output of said third latch processing after the completion of a stall in the first pipeline processing; and selecting the processing result in said second pipeline processing, when said first pipeline processing has not stalled. Column 13, lines 14-35 show that when the first pipeline is stalled,

the aforementioned third latch stores the data to be transmitted to it and when the stall is complete, the selector selects the data from the latch and transmits it to the first pipeline.

d. One can see that from figures 4 and 7 of Gearty, the data from the second pipeline is being sent or forwarded to the first pipeline. Thus, the first pipeline does not have to retrieve this data from memory or calculate it. Hennessy has shown on page 445 in the bottom paragraph that this forwarding allows for the retrieval of a missing or needed item early. The ability to retrieve a data item early in order to save time as taught by Hennessy would have motivated one of ordinary skill in the art to change the design of Sanders to use the forwarding methodology taught by Gearty.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Sanders to include the data-forwarding scheme taught by Gearty so that data items may be received early in order to save time as taught by Hennessy.

Response to Arguments

27. Applicant's arguments filed 14 February 2005 have been fully considered but they are not persuasive.

28. Applicant has argued that Sanders does not teach or suggest "control signals having timings capable of being individually controlled" as recited in claim 1 because Sanders describes only one type of control input which is applied to both the execution unit and the memory management unit. The Examiner asserts that though the origin of the control signals for the execution unit and memory management units is the same

(i.e. signal 28) and the values may initially be the same when split to the two units, the fact that the signal 28 is split defines the existence of two control signals, which are then separately and individually controlled in the following stages as shown in figure 12.

29. Applicant has also argues that Sanders does not teach or suggest "a first latch portion configured to latch said control signal inputted to each stage with a predetermined clock, said first latch portion having a plurality of flip-flops which are provided corresponding to the respective control signals and latch the corresponding control signal; and a second pipeline processing portion, disposed separately from said first pipeline processing portion, configured to perform the processing in each stage based on the control signal latched by said first latch portion" as recited in claim 1 since Sanders operates depending on the timing of the common control input 28. Figure 12 clearly shows that the control input 28 is latched based on a clock signal (which is inherently predetermined, that is determined before it is asserted) in each stage. Thus operation, while dependent on the data of the control signals originating from signal 28, is dependent on the timings of the clock signals. In certain stages such as segment 4 the clock signals are shown to be separate and different. Since the latch is timed according to a clock signal, the latch is a flip-flop. Thus the limitations of claim 1 are disclosed.

Conclusion

30. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the

claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (571) 272-4166 after October 12th and (703) 305-7305 before October 12th. The examiner can normally be reached on M-F 6:45-4:15 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane F Gerstl
Examiner
Art Unit 2183

SFG
March 18, 2005

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100